AMENDMENT TO THE CLAIMS

1. (Currently Amended) IC-circuit construction where the circuit is partitioned into power consuming sub-circuits ~~(1,6)~~ which each has to receive a supply voltage, and where the sub-circuits ~~(1,6)~~ are connected in series and where a control-circuit ~~(4)~~ is provided in order to balance the voltage drops across the power consuming sub-circuits ~~(1,6)~~ whereby constant voltage-drops over the sub-circuits ~~(1,6)~~ are maintained, and where ground voltage level (VHH) in the power supply of a first sub-circuit ~~(1)~~ is used as the supply voltage level in a second sub-circuit ~~(6)~~ and where the control circuit ~~(4)~~ comprises a first buffer capacitor ~~(10)~~ coupled in parallel over the supply voltage level (VBB) and ground voltage level (VHH) of the first sub-circuit ~~(1)~~ and a second buffer capacitor ~~(11)~~ coupled in parallel over the supply voltage level (VHH) and the ground voltage level (GND) of the second sub-circuit ~~(6)~~, whereby means for maintaining a uniform voltage drop over the first ~~(10)~~ and the second ~~(11)~~ buffer capacitor comprises at least one bucket capacitor ~~(20,21,22)~~ which is alternately coupled in parallel over the first ~~(10)~~ and the second ~~(11)~~ buffer capacitor through a switching system controlled by a toggling signal.

2. (Currently Amended) IC circuit as claimed in claim 1, wherein there are two bucket capacitors ~~(21,22)~~ that get switched at the same time such as to alternately couple to the first and the second buffer capacitor respectively.

3. (Currently Amended) IC circuit as claimed in claim 1 or 2, wherein the switches ~~(25,28,35,36,37,38)~~ for alternately coupling the bucket capacitors ~~(20,21,22)~~ are controlled by a free-running oscillator ~~(17)~~, a clock, or some other suitable signal of periodic or nonperiodic nature.

4. (Currently Amended) IC-circuit as claimed in claim 1, wherein sub-circuits ~~(1,6)~~ are digital or analog or mixed signal circuits.

5. (Currently Amended) IC circuit as claimed in claim 1, whereby sub-circuits ~~(1,6)~~ are located on each their chip.

6. (Currently Amended) IC circuit as claimed in claim 1, whereby the control circuit ~~(4)~~ is designed such as to maintain different voltage drops across sub-circuits ~~(1,6)~~.